Superconducting Digital Electronics Based on Single Flux Quantum

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Single flux quantum (SFQ) logic circuits, in which a single flux quantum is used for an information carrier, have a possibility to open a new digital system operated with over 100 GHz clock frequencies at extremely low power dissipations. Recently, much progress in basic technologies for designing SFQ circuits and operating circuits with high speeds has been done. By taking advancements in these designing tools, circuits including more than several thousands junctions easily operated with the clock frequency of more than several tens GHz. Applications of SFQ circuits such as high performance computers, high end router and high end servers are being developed in the world taking advantages of the high through-put nature and the low power dissipation of the SFQ logic.

PACS numbers: 85.25.Hv

I. INTRODUCTION

Digital circuits based on single flux quantum (SFQ) are intensively researched as a future high performance digital system. SFQ circuits can be operated with high clock rates up to 100GHz at an extremely low power dissipation. In order to assure stable operations of SFQ circuits, developing designing technology is an important issue. The optimization of circuit parameters is inevitably needed to widen operating margins. The cell-based design can ease the burden paid for designing large scale circuits. Usefulness of these designing tools for operation of SFQ circuits is demonstrated by operating chips with LSI levels. On-chip-test system to evaluate speeds of circuits are designed and circuits are operated at high clock rates.

II. DESIGN METHOD FOR SFQ LOGIC CIRCUITS

II-1. Optimization of Circuit Parameters

In order to assure stable operation of SFQ circuits, it is important to optimize values of circuit elements to widen operating margins. So far, several methods for the optimization of SFQ circuits have been proposed. These methods are divided into two categories in respect of what is used as a measure of the operating region.

One method is to improve yields, which is the rate of the number of the circuit operating correctly in all fabricated circuits. The method of inscribed hyper-spheres and the center of gravity method are well known as optimization methods to improve yield [1].
These methods well represent parameter spread which arises from the fabrication process. The disadvantage is the computational cost is large.

The other is to enlarge the critical margin [2]. The critical margin is the narrowest margin when other parameters are kept in initial values. An advantage of the critical margin method is relatively low computational cost. However, an optimized parameter sometimes falls into local minimum conditions.

To improve the critical margin method, a new optimization procedure are proposed, in which Monte-Carlo method is introduced to avoid falling local minimum and global spread of circuit parameters are taken into account [3]. As the first step, Monte-Carlo method introduced the critical margin method in order to reduce the effect of initial values of parameters. Monte-Carlo method creates various parameters around initial parameters.

Fig. 1 shows the first step optimization procedure for a two dimensional case. Initial values are normalized to be $X = Y = 1$ (a). The closed curve (b) represents the region in which the circuit operates correctly. Monte-Carlo method makes circuit parameters scatter around initial values. The region where data are scattered is indicated by a square in Fig. 1. Typically, 50 sets of the circuit parameters are created. Then, the critical margin method is applied to each set. A calculated parameter for one of the parameter sets is illustrated in Fig. 1 as a point (c). In the critical margin method, margins of all parameters have to be calculated. For example, in calculation of the margin $X$, the parameter $Y$ is kept to $Y_1$ and the value of $X$ is changed from 0 to 2, checking whether the circuit operates correctly or not. The margin of the parameter $Y$ is calculated as well as the parameter $X$. In this case, the critical margin of the parameter $Y$ does not exist so that the value of the parameter $X$ is changed to the center of the operating region (d). Again margins of the parameter $X$ and $Y$ are calculated. Then, the value of the parameter $Y$ is determined so
as the critical margin is maximum, hence, centering the operating point in the operating region (e). Similar optimization is carried out for the other parameter sets produced by Monte-Carlo method. Finally, a circuit with a circuit parameter set to have the biggest critical margin is chosen as an optimized circuit.

To increase the reliability of the optimization, global parameter spreads are taken into account. The global spread means spread occurs in the run-to-run process. For example, if all Josephson critical currents increased or decreased by 10% from the designed value, the critical margin method is adopted so as to maximize margins, determining the parameter set as the optimized one.

Usefulness of this optimization method is experimentally verified by measuring bias margins of fabricated circuits. As an example, optimization of a T-FF circuit is shown.
TABLE I: Experimental results. Only circuits after optimization are operated at designed points.

<table>
<thead>
<tr>
<th></th>
<th>Designed value [µA]</th>
<th>Bias margin</th>
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<tbody>
<tr>
<td>before optimization</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Buffer</td>
<td>200</td>
<td>−79%~+14%</td>
</tr>
<tr>
<td>T-FF</td>
<td>180</td>
<td>+17%~+50%</td>
</tr>
<tr>
<td>AJTL</td>
<td>200</td>
<td>+105%~+120%</td>
</tr>
<tr>
<td>after optimization</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Buffer</td>
<td>140</td>
<td>−59%~+143%</td>
</tr>
<tr>
<td>T-FF</td>
<td>160</td>
<td>−28%~+69%</td>
</tr>
<tr>
<td>AJTL</td>
<td>110</td>
<td>−32%~+191%</td>
</tr>
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</table>

Fig. 2 shows the equivalent circuit of the T-FF circuit. The circuits before and after optimization are fabricated by using the Nb junction technology with the current density of 2.5 KA/cm². Fig. 3 show the photograph of the circuit.

Measured bias margins are shown in Table I. Bias margins after the optimization are larger than those before optimization even though the global average critical current spread is +18%. Moreover, only the circuit after the optimization can be operated at the designed bias current.

A new optimization procedure to use the critical margin method combined with Monte-Carlo method is proposed. The usefulness of this optimization method are demonstrated by measuring the bias margins in unoptimized and optimized circuits.

II-2. Cell Based Design

As the integration scale is getting larger, development of CAD (Computer-Aided-Design) tools is a matter of great importance. Since SFQ logic system is completely different from semiconductor one, CAD’s developed for semiconductor LSI’s are difficult to use for designing SFQ circuits. It is important to develop design tools for SFQ LSI.

1 Cell Based Design Tool has been developed by CONNECT (Cooperation of Nagoya University, NEC, CRL, and Yokohama National University Team) team in Japan.
One of the approaches is the cell based design [4] which allows us to design circuits in a top down manner. A circuit is composed of cells. Each cell is optimized and leak currents to neighboring cells are minimized.

About 100 cells are designed and installed in a library, operating by the CAD of the Cadence Design System Inc. Each cell has data of three levels, a digital level, an analog level, and a layout level. In digital level, each cell defined by the Verilog hardware description language, containing the logical operation, the delay time, the setup time, and the hold time. The digital simulation is performed by using these informations, including timing simulations.

In the analog level, circuit parameters of cells composed of Josephson junctions, inductances and resistances are optimized by the method as described in the previous section. In the analog level simulation, timing information such as delay time, setup time, and hold time can be obtained, connecting to the digital level.

The layout level contains informations about circuit patterns or layouts. Layout composed of an unit area of 40 $\mu$m $\times$ 40 $\mu$m square. Fig. 4 shows an example of a cell layout.

The cell based design allows us to make design circuits in a top-down manner preparing data of those three layer levels. A logic circuit is composed schematically by logic gates from the cell library. In this stage, timing simulations are performed using the digital level by checking whether the operation is correct or not. By changing lengths of JTL’s (Josephson transmission Line), timing is controlled so as to maximize the operating margin.

Moreover, since data of a circuit as a combination of cells can be the source file of the JSIM, the bias margin of the circuit is checked by making the analog simulation at the last stage. Fig. 5 shows an example of the schematic and layout view of a designed circuit.

The development of the CAD system with the cell library consisting of three level data, i.e., the digital, the analog, and the layout levels, makes it possible to design circuits in the top-down manner which is inevitably needed to design a large scale circuit with a high complexity. Further researches of CAD’s with increased functions for SFQ logic circuits, i.e., automatic placing and routing are being done.

III. HIGH SPEED OPERATIONS OF SFQ CIRCUITS

III-1. On-Chip Test System

It is important to know how high the speed of the circuit is. In general, SFQ circuits are operated with the clock frequency of more than 50 GHz. However, measuring apparatuses and clock generators operated such high frequencies are not available. In order to solve this problem, the on-chip test system is developed, in which a high frequency clock generator and interfaces are integrated on the same chip on a circuit under test. Fig. 6 shows the schematic diagram of the on-chip test system. The on-chip test system consists of shift registers and a high frequency clock generator. Digital data are written in a shift register with a slow clock rate. Then, the high frequency clock generator is triggered to send clocks with a high frequency to the circuit. The high frequency operation is performed
and the result is written in another shift register. The result is read by a clock with a slow late from the shift register to know whether the circuit is operated correctly or not. The clock generator composed of a ladder circuit generates a pulse train. The frequency of the clock generator is calculated by the data of bias currents.

**III-2. High Frequency Operation**

By taking advances of the designing technology of SFQ circuits, a number of circuits are operated with high frequency clocks. In Table II, circuits demonstrated so far are summarized.

**IV. CONCLUSIONS**

Much progress in fundamental technology such as design and measurement technologies of SFQ circuits has been made as described above. By taking these progresses, applications of SFQ logics have been being developed.
TABLE II: On chip test results for various SFQ circuits

<table>
<thead>
<tr>
<th>Circuits</th>
<th>Number of JJ</th>
<th>Operating Frequency (GHz)</th>
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<tbody>
<tr>
<td>T1-Cell Half-Adder</td>
<td>500</td>
<td>43</td>
</tr>
<tr>
<td>Carry-Save Serial Adder</td>
<td>630</td>
<td>14</td>
</tr>
<tr>
<td>M-Code Generator</td>
<td>400</td>
<td>17.5</td>
</tr>
<tr>
<td>8bit Shift Register</td>
<td>450</td>
<td>55</td>
</tr>
</tbody>
</table>

Wide band analog to digital converters, high speed switch for high-end routers and microprocessors for high performance computers are considered as most suitable applications of SFQ logic circuits. Intensive developments are being done in the world and it is expected to be realized as products in the market place in the near future.

References